REMARKS / ARGUMENTS

This Amendments and Response to Office Action is filed in response to the Office Action of March 1, 2005.

The disclosure was objected to because no description for the newly added Fig. 5B was found in the specification. Additionally, the specification was not amended to address the change of Fig. 5 to Fig. 5A.

Claims 1, 11, 15, and 16 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,433,582 issued to Hirano ("Hirano"). Moreover, claims 2, 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano in view of U.S. Patent No. 5,917,339 issued to Kim ("Kim"). Claims 4-9 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano in view of Kim and further in view of U.S. Patent No. 6,249,145 Tanaka *et al.* ("Tanaka *et al.*"). Claims 8 and 9 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano in view of Tanaka *et al.* Moreover, claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano in view of Tanaka *et al.*

With entry of the above amendments and consideration of the reasons stated below, applicants respectfully submit that the objections and rejections set forth in the outstanding Office Action are overcome.

I. Objection of the specification

The amendment to the specification describes the newly added Fig. 5B as well as the change of Fig. 5 to Fig. 5A. Applicants submit that the objection has been overcome, and its withdrawal is respectfully requested.

II. Rejection of Claims 1, 11, 15, and 16 under 35 U.S.C. 102(e) as being anticipated by Hirano

The subject application is directed to overcome the drawbacks of conventional level shifter circuitries when the voltage difference between the shifted signals is relatively large. According to the subject application, the device sizes of both the PMOS and NMOS transistors in the basic shifter are fabricated of comparable physical scales. To accomplish the above objective, with reference to Figs. 2 and 3 of the subject application, the dynamic CMOS level shifter circuit apparatus uses a power-down control signal (PWD) at the gate terminal 231 of the PMOS transistor 230 for a specified period of time during operation. More particularly, when the input signal changes state such as from a high state to a low state, the PWD is applied for a predetermined period of time. The PWD will cut off the power supplied to the PMOS transistors 211 and 221 in Fig. 2 until the NMOS transistors 212 and 222 shown in Fig. 2 settle their state transition.

Hirano disclosed a level shift circuit comprising a basic level shift circuit (P1, P2, N1, N2) and a PMOS transistor PR1. As shown in Figs. 2 and 3 of Hirano, a signal ATD is applied with a voltage level Vvv to the gate of the PMOS transistor PR1 **before** the input signal Si is fallen from a high state Vcc to a low state Vss. The signal ATD with voltage level Vvv reduces the current driving ability of the PMOS transistor PR1. Therefore, the electrical resistance between the node T4 and the node nd4 is increased, and the voltage at node nd4 is reduced in order to **turn on** the transistor P1. *See* Hirano, Col. 8, lines 4-22.

Hirano fails to teach the particular feature "the power-down control signal being changed to a high state for a predetermined period **when** the signal from the first logic family changes

state" and "the power-down control signal controls the gate terminal of said power-down control PMOS transistor **to cut off the power to said first and second PMOS transistors** for a duration of time sufficient for said first and second NMOS transistors to settle state transition," as recited in claim 1 of the subject application. Moreover, Hirano fails to teach "the first transistor **cuts off** the connection between the level shift unit and the power terminal **when** the voltage level of the input terminal of the level shift unit changes," as recited in claim 11 of the subject application. In other words, Hirano does not disclose a power supplied to a basic level shift circuit being cut off at the moment when the voltage level of the input terminal of the level shift unit changes. For at least these reasons, it is submitted that the anticipation rejection for claims 1 and 11 is inadequate, and its withdrawal is respectfully solicited.

By virtue of their respective dependency upon claim 11, dependent claims 15 and 16 also patently define over the prior art reference.

III. Rejection of claims 2, 3 and 17 under 35 U.S.C. 103(a) as being unpatentable in view of Hirano and Kim

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skills in the art, to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success to combine the teachings of the references. Finally, the prior art reference (or references when combined) must teach or suggest all the claimed elements. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art references and not based on applicant's disclosure. *See* MPEP §706.02(j).

Hirano fails to and does not even suggest using two inverters to provide complementary outputs. The two inverters in 15 and 16 in Kim function to buffer the output from block 14 rather than providing complementary outputs. Moreover, the combination of these two patents also fails to teach "the power-down control signal being changed to a high state for a predetermined period when the signal from the first logic family changes state" and "the power-down control signal controls the gate terminal of said power-down control PMOS transistor to cut off the power to said first and second PMOS transistors for a duration of time sufficient for said first and second NMOS transistors to settle state transition," as recited in the independent claims 2, 3 and 17. For at least these reasons, it is submitted that the obviousness rejection is inadequate, and its withdrawal is respectfully solicited.

IV. Rejection of claims 4-9 and 18-20 under 35 U.S.C. 103(a) as being unpatentable in view of Hirano, Kim and Tanaka *et al.*

The combination of these three patents also fails to teach the features of the independent claims upon which claims 4-9 and 18-20 depend. More particularly, none of these three patents teaches the use of an additional POMS transistor cascaded between the power terminal and the PMOS transistor 230. For at least these reasons, it is submitted that the obviousness rejection is inadequate, and its withdrawal is respectfully solicited.

V. Rejection of claims 8 and 9 under 35 U.S.C. 103(a) as being unpatentable in view of Hirano and Tanaka *et al.*

The combination of these two patents also fails to teach the features of the independent claims upon which claims 8 and 9 depend. More particularly, none of these three patents

teaches the use of an additional POMS transistor cascaded between the power terminal and the PMOS transistor 230. For at least these reasons, it is submitted that the obviousness rejection is inadequate, and its withdrawal is respectfully solicited.

VI. Rejection of claim 10 under 35 U.S.C. 103(a) as being unpatentable in view of Hirano

Hirano fails to teach the feature "the power-down control signal being changed to a low state for a predetermined period of time **when** the signal from the first logic family changes state" and "the power-down control signal controls the gate terminal of said power-down control NMOS transistor to **cut off the power to** said first and second NMOS transistors." For at least these reasons, it is submitted that the obviousness rejection is inadequate, and its withdrawal is respectfully solicited.

VII. Rejection of claims 12-14 under U.S.C. 103(a) as being unpatentable in view of Hirano and Tanaka *et al.*

For the same reasons stated above, the withdrawal of this rejection is respectfully solicited.

CONCLUSION

For at least the foregoing reasons, it is believed that all of pending claims 1-8 and 10-20 of the present application patently define over the prior art references and are in proper condition for allowance. Furthermore, because no new claim is added, no additional fees are required. In the event, however, that additional fees are required to complete this filing, Commissioner is

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authorized to deduct any deficiencies from Deposit Account 13-0480, Attorney Docket No. 87157656.242004.

If the Examiner has any questions regarding this filing or the application in general, the Examiner is invited to contact Applicant's attorney at the below-listed telephone number.

Respectfully submitted,

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